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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,297	12/12/2001	Koji Morita	FY.17451US0A	1699
20995	7590 03/11/2003			
KNOBBE MARTENS OLSON & BEAR LLP			EXAMINER	
2040 MAIN S' FOURTEENT	H FLOOR	LEWIS, MONICA		
IRVINE, CA 92614			ART UNIT	PAPER NUMBER
			2822	
			DATE MAILED: 03/11/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary Examiner Art Unit Bonica Lewis Art Unit 2822 The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).	_		Application N	TA			
Examiner Montico Lewis 2822			Application No.	Applicant(s)			
Monica Lewis - The MAILING DATE of this communication appears on this covir is sheet with the correspondence address → Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. THE MAILING DATE OF THIS COMMUNICATION. If the period for reply specified store is last han thisy (30) days, a reply within the standary minimum of thiny (30) days with the considered timely. If the period for reply specified store is last han thisy (30) days, a reply within the standary memory and of the provision of the period for reply specified store is the standary period with again and the period for reply specified store is the standary sender all again with eight sets (30) days with the considered timely. If the period for reply specified store is the standary sender all again with eight sets (30) days will be considered timely. If the period for reply specified sets is the standary sender all agains and is set in the standary set and senders and the set in the period of the communication, even if brindly filed, may reduce any search grade the set of the communication. Sets the set of the communication is the set of the standary reply sets of the communication, even if brindly filed, may reduce any search grade the set of the set of the set of the standary reply sets of the set of th			10/022,297	MORITA ET AL.			
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THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be waited used the provision of 37 CPR 1.15(8). In no event, however, may a reply be limitely fled after SX (8) MONTHS from the mailing date of this communication. It NO period for reply is specified above, the maximus abstratory pelow will mis the station of misconnection of the communication. Fallule to reply within the set of extended period for reply will, by statutory misconnection, over if firely 100 days will be considered imaging. Any reply receive by the Office text he liver amonths after the mailing date of this communication, over if firely filed the may reduce any service by the office text he liver amonths after the mailing date of this communication, over if firely filed the may reduce any service by the office text he liver amonths after the mailing date of this communication. Any reply receive by the Office text he liver amonths after the mailing date of this communication. This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1 and 4-32 is/are pending in the application. 4a) Of the above claim(s) 27-32 is/are withdrawn from consideration. 5) Claim(s) 1.4-7 and 13-26 is/are rejected. 7) Claim(s) 1.4-7 and 13-26 is/are rejected. 7) Claim(s) 1.4-7 and 13-26 is/are rejected. 7) The drawing(s) filed on is size and accepted or bim objected to by the Examiner. Application Papers 9) The drawing(s) filed on is size as a complete or provided to be provided to by the Examiner. 10) The drawing(s) filed on is size as a complete or provided to the drawing as a complete or provided to the drawing and provided to the drawing as a complete or provided to the drawing and provided to the provided to the drawing as a complete or provided to the drawing as a complete or provided to the provided to the p			lears on the cover sneet with the c	correspondence address			
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	2) Notic	e of Draftsperson's Patent Drawing Review (PTO-948)	5) Notice of Informal				

DETAILED ACTION

1. This action is in response to the amendment filed December 18, 2002.

Response to Arguments

2. Applicant's arguments with respect to claims 1 and 4-26 have been considered but are moot in view of the new ground(s) of rejection.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

Claim Rejections - 35 USC § 112

- 4. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 5. Claims 8-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "a coefficient of expansion of the synthetic resin being generally less than a coefficient of expansion of the substrate or a coefficient of expansion of the land and being generally greater than the other one of the coefficient of expansion of the substrate and the coefficient of expansion of the land" (See

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Claim 8). Claims 9-12 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 16-19, 21, 23 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagisawa (Japanese Patent No. JP63213936).

In regards to claim 16, Yanagisawa et al. ("Yanagisawa") discloses the following:

a) a substrate (1), a land (2) formed on the substrate, a semiconductor chip (6) mounted on the land, a solder layer (4) joining the semiconductor chip with the land, the semiconductor chip defining at least two corners positioned generally opposite to each other, the land defining at least two corners disposed in proximity to the corners of the semiconductor chip (See Abstract and Figure b).

In regards to claim 17, Yanagisawa discloses the following:

a) corners of the land are the closest portions to the corners of the semiconductor chip (See Figure b).

In regards to claim 18, Yanagisawa discloses the following:

a) the semiconductor chip is generally configured as a rectangular shape (See Figure b).

In regards to claim 19, Yanagisawa discloses the following:

a) the semiconductor chip defines four corners, and the land defines four corners corresponding to the corners of the semiconductor chip (See Figure b).

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In regards to claim 21, Yanagisawa discloses the following:

a) land is generally configured as a rectangular shape except for the corners (See Figure b).

In regards to claim 23, Yanagisawa discloses the following:

a) area of the land is larger than an area of the semiconductor chip, and the area of the land generally shrinks toward the corners of the semiconductor chip (See Figure b).

In regards to claim 24, Yanagisawa discloses the following:

a) area of the land is larger than an area of the semiconductor chip, and the area of the land generally expands from the corners of the semiconductor chip (See Figure b).

Claim Rejections - 35 USC § 103

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 9. Claims 1, 4 and 13 are rejected under 35 U.S.C. 103(a) as obvious over Ichiyama (U.S. Patent No. 5,373,190) in view of Applicant's Prior Art and Yanagisawa (Japanese Patent No. 63213936).

In regards to claim 1, Ichiyama discloses the following:

a) a substrate (11), a land (9) formed on the substrate, a semiconductor chip (1A) mounted on the land, a solder layer (12) only through which the semiconductor chip is joined with the land, and a synthetic resin (4) covering the semiconductor chip on the substrate (See Figure 3).

In regards to claim 1, Ichiyama fails to disclose the following:

a) resin covering the land and solder layer.

However, Applicant's Prior Art discloses resin covering the land and solder (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyamato to include resin covering the land and solder as disclosed in Applicant's Prior Art because it aids in protecting the device from malfunctioning (See Paragraph 3).

Additionally, since Ichiyama and Applicant's Prior Art are both from the same field of endeavor, the purpose disclosed by Applicant's Prior Art would have been recognized in the pertinent art of Ichiyama.

b) a coefficient of expansion of the synthetic resin being generally less than a coefficient of expansion of the substrate or a coefficient of expansion of the land.

However, Yanagisawa discloses an aluminum substrate and silicon resin (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyamato to include an aluminum substrate and silicon resin as disclosed in Yanagisawa because it aids in providing a high reliability circuit (See Abstract).

Additionally, since Ichiyama and Yanagisawa are both from the same field of endeavor, the purpose disclosed by Yanagisawa would have been recognized in the pertinent art of Ichiyama.

In regards to claim 4, Ichiyama discloses the following:

a) a substrate (11), a land (9) formed on the substrate, a semiconductor chip (1A) mounted on the land, a solder layer (12) only through which the semiconductor chip is joined with the land, and a synthetic resin (4) covering the semiconductor chip on the substrate (See Figure 3).

In regards to claim 4, Ichiyama fails to disclose the following:

a) resin covering the land and solder layer.

However, Applicant's Prior Art discloses resin covering the land and solder (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyamato to include resin covering the land and solder as disclosed in Applicant's Prior Art because it aids in protecting the device from malfunctioning (See Paragraph 3).

Additionally, since Ichiyama and Applicant's Prior Art are both from the same field of endeavor, the purpose disclosed by Applicant's Prior Art would have been recognized in the pertinent art of Ichiyama.

b) a coefficient of expansion of the synthetic resin being generally less than a coefficient of expansion of the substrate or a coefficient of expansion of the land.

However, Yanagisawa discloses an aluminum substrate and silicon resin (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyamato to include an aluminum substrate and silicon resin as disclosed in Yanagisawa because it aids in providing a high reliability circuit (See Abstract).

Additionally, since Ichiyama and Yanagisawa are both from the same field of endeavor, the purpose disclosed by Yanagisawa would have been recognized in the pertinent art of Ichiyama.

In regards to claim 13, Ichiyama discloses the following:

a) the semiconductor chip defines at least two corners positioned generally opposite to each other, the land defines at least two corners in proximity to the corners of the semiconductor chip (See Figure 3).

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10. Claim 6 is rejected under 35 U.S.C. 103(a) as obvious over Ichiyama (U.S. Patent No. 5,373,190) in view of Applicant's Prior Art, Yanagisawa (Japanese Patent No. 63213936) and Shin et al. (U.S. Patent No. 5,844,305).

In regards to claim 6, Ichiyama fails to disclose the following:

a) land comprises copper.

However, Shin et al. ("Shin") discloses a copper land (See Column 1 Lines 47-49). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyama to include a copper land as disclosed in Shin because it aids in increasing the overall speed of the circuit (See Column 1 Lines 5-49).

Additionally, since Ichiyama and Shin are both from the same field of endeavor, the purpose disclosed by Shin would have been recognized in the pertinent art of Ichiyama.

11. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as obvious over Ichiyama (U.S. Patent No. 5,373,190) in view of Applicant's Prior Art, Yanagisawa (Japanese Patent No. 63213936) and Nippon (Japanese Publication No. JP53143656A).

In regards to claim 5, Ichiyama fails to disclose the following:

a) the coefficient of the linear expansion of the synthetic resin is generally less than approximately 23 ppm/K.

However, Nippon discloses a synthetic resin that includes epoxide (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyama to include a synthetic resin that includes epoxide as disclosed in Nippon because it aids in increasing the moisture resistance and mechanical strength (See Abstract).

Additionally, since Ichiyama and Nippon are both from the same field of endeavor, the purpose disclosed by Nippon would have been recognized in the pertinent art of Ichiyama.

In regards to claim 7, Ichiyama fails to disclose the following:

a) synthetic resin includes epoxide.

However, Nippon discloses a synthetic resin that includes epoxide (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyama to include a synthetic resin that includes epoxide as disclosed in Nippon because it aids in increasing the moisture resistance and mechanical strength (See Abstract).

Additionally, since Ichiyama and Nippon are both from the same field of endeavor, the purpose disclosed by Nippon would have been recognized in the pertinent art of Ichiyama.

12. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as obvious over Ichiyama (U.S. Patent No. 5,373,190) in view of Applicant's Prior Art, Yanagisawa (Japanese Patent No. 63213936) and Yamanashi (Japanese Patent No. JP02000253570A).

In regards to claim 14, Ichiyama fails to disclose the following:

a) the semiconductor chip controls electric power.

However, Yamanashi discloses a chip that controls power (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyama to include a chip that controls power as disclosed in Yamanashi because it aids in preventing damages to the motor controller (See Abstract).

Additionally, since Ichiyama and Yamanashi are both from the same field of endeavor, the purpose disclosed by Yamanashi would have been recognized in the pertinent art of Ichiyama.

In regards to claim 15, Ichiyama fails to disclose the following:

a) the semiconductor chip controls power of an electric motor arranged to drive an electric vehicle.

However, Yamanashi discloses a chip that controls power (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ichiyama to include a chip that controls power as disclosed in Yamanashi because it aids in preventing damages to the motor controller (See Abstract).

Additionally, since Ichiyama and Yamanashi are both from the same field of endeavor, the purpose disclosed by Yamanashi would have been recognized in the pertinent art of Ichiyama.

13. Claims 20, 22 and 26 are rejected under 35 U.S.C. 103(a) as obvious over Yanagisawa et al. (Japanese Patent No. JP63213936).

In regards to claim 20, Yanagisawa fails to disclose the following:

a) at least a length of a shorter side of the rectangular shape is longer than approximately 2.5 millimeters.

However, the applicant has not established the critical nature of the dimension of 2.5 millimeters. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

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In regards to claim 22, Yanagisawa fails to disclose the following:

a) a round shape except for the comers.

Although Yanagisawa does not specifically disclose a round land, a land in another shape is disclosed. It is a design choice to have a round land. The round land functions the same as a land of another shape.

In regards to claim 26, Yanagisawa fails to disclose the following:

a) semiconductor chip is joined with the land in a reflow soldering method.

However, the limitation of "reflow soldering method" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao and Sato et al., 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also In re Brown and Saffer, 173 USPQ 685 (CCPA 1972): In re Luck and Gainer, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and In re Marosi et al., 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

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14. Claim 25 is rejected under 35 U.S.C. 103(a) as obvious over Yanagisawa et al. (Japanese Patent No. JP63213936) in view of Yamanashi (Japanese Patent No. JP02000253570A).

In regards to claim 25, Yanagisawa fails to disclose the following:

a) the semiconductor chip controls electric power.

However, Yamanashi discloses a chip that controls power (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yanagisawa to include a chip that controls power as disclosed in Yamanashi because it aids in preventing damages to the motor controller (See Abstract).

Additionally, since Yanagisawa and Yamanashi are both from the same field of endeavor, the purpose disclosed by Yamanashi would have been recognized in the pertinent art of Yanagisawa.

Allowable Subject Matter

15. Claims 8-12 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Conclusion

16. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Christie et al. (U.S. Patent No. 5,668,059) discloses a solder interconnection structure; and b) Kober et al. (U.S. Patent No. 5,793,150) discloses a flat seal.

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17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML March 6, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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